DETAILED REMARKS

The OA of 10/14/2005 rejected all claims of the present invention as anticipated by Luk et al, Pat. No. 6,768,692 (Luk), and Wang et al, Pat. No. 6,014,338 (Wang). Applicant respectfully submits that the rejection over Luk and Wang is not warranted because applicant contends that these prior art documents fail anticipate the present invention.

Before detailing the anticipation of individual claims, applicant would like recap in a nutshell the state of the prior art of multi (sub) array Dynamic Random Access Memory (DRAM) design, the invention of the application, and the trust of the Luk and Wang disclosures.

The prior art is well summarized in the "Background of the Invention" section of Luk (col 1, lines 14 -63) and in Fig. 1A of Luk, labeled "Prior Art". With the subdivision of memory cells into arrays, there also came a hierarchical bitline and circuit structure. Everything became divided into "local", namely dealing with, belonging to, an array, and "global" belonging to multiples of arrays and to the I/O characteristics of the whole memory. Such a division has also become standard practice as far as sensing is concerned. At the array level there are the local, or first stage, or primary, (these names are interchangeable) sense amplifiers. Their number is on the same scale as that of bitlines, which can be in the millions. The tasks to handle long wires, to drive the relatively few memory I/O-s, to write and write-back data to the cells, are handled by the global – or secondary, or second stage, or main – sense amplifies, which belong not to any relatively small groups of cells, but to one or more of the memory arrays. Both the primary and secondary sense amplifiers are differential, namely they sense a voltage difference between two lines, rather the single ended type, sensing voltage of a single line. The existing state of affairs is also well put forth, for instance, in the 2001 book by Kiyoo Itoh, titled: "VLSI Memory Chip Design" (ISBN: 3540678204, Publisher: Springer-Verlag New York, Incorporated). Applicant attaches a copy of a relevant figure from this book. Figure 3.64 on page 169 of the book shows clearly the local sense amplifiers (SA) inside the memory arrays, and the global sense amplifiers (MA) outside the arrays. Thus, the prior art has <u>two sensing stages</u> (primary, global).

The present invention teaches <u>primary</u> sense amplifiers, which are special in that they are single ended, are capable to write and write-back data to the cells without global sense amplifier involvement, and are designed for high gain. Thus, the present invention involves <u>two</u>

amplifications stages in the primary sense amplifier, which is completely different from the two sensing stages of the prior art. The invention also teaches that the whole structure of the DRAM is single ended, and has wide bandwidth with no bitline address.

The invention in Luk (6,768,692) was the elimination of the primary sense amplifiers, using only global amplifiers designed for single sensing. See for instance col 2 lines 3 to 16. Accordingly, Luk has absolutely no teaching on primary sense amplifiers.

Wang (6,014,338) deals with register files and not DRAM-s. Register files are Static Random Access Memory (SRAM), see for instance col. 1 line 8, and col 3 line 24. Due to the different kind of memory cell, the issues of write, and write-back are different for SRAM-s and DRAM-s. Applicant respectfully submits that it is not clear how Wang might be relevant as DRAM prior art.

In more detail, regarding claim 1, OA states that Luk teaches "at least one primary sense amplifiers (fig. 1A, 150), wherein the least one primary sense amplifier has single ended sensing, has data storage and data write back capability, and has at least two amplification stages (col.1, line 25-45)" ; that Wang "discloses a DRAM comprising; at least one primary sense amplifiers (fig. 1, 18), wherein the least one primary sense amplifier has single ended sensing, has data storage and data write-back capability (col 2, line 34-44, having a feedback loop), and has at least two amplification stages (col.2 line 17-44);". In reply, applicant respectfully points out that Fig. 1A in Luk is "Prior Art", and, as discussed above, describes both primary and secondary amplifiers. However, the "single ended sensing, data storage and data write back capability" in Luk is all about the global sense amplifier, as it is usual in the art for global amplifiers. Luk does not teach anywhere at "least two amplification stages". Wang teaches single ended sensing for an SRAM, but nowhere is discussing write and/or write-back. In Fig. 2 Wang shows a storage latch only, but no mechanism for writing the cell. Consequently, it must be conventional art, thus not bearing on the present invention. Also, depending on the details of the latch (30, 32) the circuit may, or may not, be considered having two amplification stages, (in contrast with 2 stages of sensing, Fig. 2 plus Fig. 3 in Wang)

Applicant amended claim 1 to better express the full breadth and scope of the present invention, and maybe to diminish the potential for confusion. Applicant included into claim 1 the limitations of claim 2, namely the global sense amplifiers. In this manner claim 1, independently of the primary or secondary nomenclature, is more clearly distinguishable from Luk, where

there is only one sense amplifier in the path between the cells and the I/O-s. To clearly distinguish from Wang regarding the number of amplification stages, and regarding writing to the cell, applicant, instead of the two amplification stages, introduced the limitation of the passtransistor in the write-back path. This passtransistor, indicated 156 in the figures of the invention and discussed in several places of the specification, such as from line 21 page 9 to line 4 on page 10; line 15 page 10; line 10 page 15. Without such a passtransistor the write/write-back commands cannot be executed. Wang has not even a hint, let alone anticipation for such a device. Accordingly, applicant respectfully avers that the as amended claim 1 of the invention now is clearly and unequivocally distinguished from Luk and Wang, and thus patentable.

Claim 2 has been canceled, while claims 3 - 8 are as they were in the applicant's response of 06/28/05. Applicant respectfully contends that if independent claim 1 is patentable, then dependent claims 3 - 8 of this amendment, by introducing further limitations, are a fortiori patentable. However, a few points need to be addressed. As per claim 3, Luk and Wang does not teach small voltage swing, as per claim 6 and 7 Luk and Wang does not teach customized and/or dynamically adjusted thresholds. For dynamically adjusting thresholds body contact and bias are needed, as is shown on all transistors in figures 1, 2 and 3 of the present invention. These contacts are representatively labeled with the word "bias". Neither Luk nor Wang show any body contacts on their circuit figures.

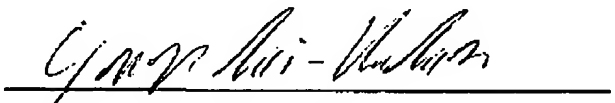
Regarding claims 9 and 21 OA states: "... Luk discloses a DRAM, comprising: ... a plurality of primary sense amplifiers (fig. 2A, 120) ... " Applicant would respectfully point out that indicating number 120 is associated with global sense amplifiers, as labeled on the figures, and described throughout the specification, for instance: col 4 lines 5 -11. In fact, as discussed earlier in this reply, the invention by Luk was precisely the elimination of the primary sense amplifiers, using only global amplifiers. Note for instance, that in the place where in the "Prior Art" Fig. 1A Luk shows primary sense amplifiers 150, the figures depicting the invention 1C, 1B, 2A, 2B show simple buffers 110, that have no sensing capability. Accordingly, Luk cannot possibly anticipate the present invention, and claims 9 and 21 as they stand after the examiner's amendment, are novel and patentable. Furthermore, all non-canceled dependent claims that depend on independent claims 9 and 21 by introducing further limitations, are a fortiori patentable.

CLOSING STATEMENTS

Applicant respectfully submits that as expressed in this amendment the application now claims only patentable subject matter.

Applicant further submits that this application is now in condition for allowance, which action is respectfully requested.

Respectfully,



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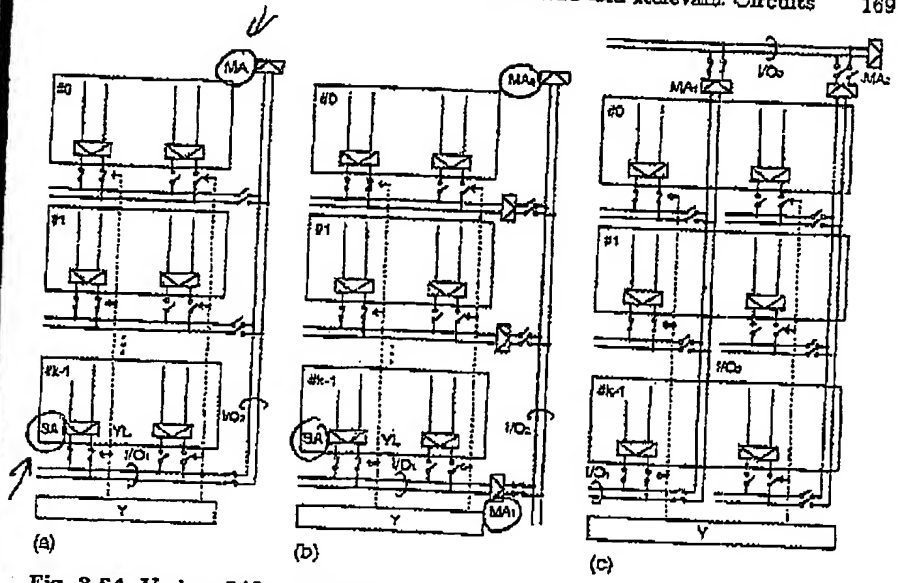

Fig. 3.64. Various I/O configurations [3.4, 3.46]. Y, column decoders and drivers. (a) Two kinds of I/Os; (b) two kinds of I/Os with MA; (c) three kinds of I/Os

(Al_2). Note that each word line is shunted with the first-level aluminum layer (Al_1). Obviously, the sub-I/O capacitance can be reduced without any area penalty, although the number of I/O_2 lines increases with the number of I/O_1 divisions. Thus, a sense amplifier can directly drive both sub-I/O_1 and I/O_2 lines at a high speed. Since MA_1 drives the lightly capacitive I/O_3 line quickly, the total speed is improved. The following are comparisons between the above three configurations, exemplified by a 1 Mb array of 2048 word lines at a 3 μm pitch and 512 pairs of data lines at a 7 μm pitch [3.46]. For configuration (a), the I/O_1 and I/O_2 capacitances are 2.3 pF and 0.9 pF, respectively, while for configuration (c) they are 0.6 pF and 0.9 pF for four I/O_1 divisions. Thus, the total capacitance that a sense amplifier must drive is 3.5 pF for (a), 2.6 pF for (b), and 1.8 pF for (c) as a result of adding a data-line capacitance of 0.3 pF. Therefore, configuration (c) achieves the fastest speed. Here, the chip area of (c) is smaller than that of (b) because the number of MA_1's is eight for (b) and four for (c).

The hierarchical I/O configuration in Fig. 3.64c has become increasingly important with increasing memory capacity, because it provides high-speed and beneficial functions without an area penalty. There has been a proposal for a 64 Mb chip [3.41], in which an I/O_2 line (Al_2) of 9.5 mm length runs along the word-line shunted region. Moreover, a parallel architecture for a 64 Mb chip [3.47], to increase the throughput or to shorten the testing time,